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INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 19667-0011	**FOR FURTHER ACTION**	See Form PCT/IPEA/416
International application No. PCT/US2005/006006	International filing date *(day/month/year)* 23.02.2005	Priority date *(day/month/year)* 23.02.2004

International Patent Classification (IPC) or national classification and IPC
INV. H05K1/16 H05K3/46

Applicant
GEORGIA TECH RESEARCH CORPORATION et al.

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 5 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. ☒ *sent to the applicant and to the International Bureau)* a total of 23 sheets, as follows:
      - ☒ sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      - ☐ sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.

   b. ☐ *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or tables related thereto, in electronic form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

☒	Box No. I	Basis of the report
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☒	Box No. VIII	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
27.09.2005	20.06.2006
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Batev, P Telephone No. +49 89 2399-7970

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/US2005/006006

Box No. I Basis of the report

1. With regard to the **language**, this report is based on

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of:
   - ☐ international search (under Rules 12.3(a) and 23.1(b))
   - ☐ publication of the international application (under Rule 12.4(a))
   - ☐ international preliminary examination (under Rules 55.2(a) and/or 55.3(a))

2. With regard to the **elements*** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

Description, Pages

1, 2, 4-11, 13-31, 33, 39, 40, 42-47, 49, 50	as originally filed
32, 34, 48	filed with telefax on 27.09.2005
3A, 3B, 12, 35-38, 41	filed with telefax on 08.05.2006

Claims, Numbers

1-24	filed with telefax on 08.05.2006

Drawings, Sheets

1/37-17/37, 24/37, 26/37-37/37	as originally filed
18/37-23/37, 25/37	filed with telefax on 08.05.2006

☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing

3. ☐ The amendments have resulted in the cancellation of:
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

* *If item 4 applies, some or all of these sheets may be marked "superseded."*

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-24
	No:	Claims	none
Inventive step (IS)	Yes:	Claims	1-24
	No:	Claims	none
Industrial applicability (IA)	Yes:	Claims	1-24
	No:	Claims	none

2. Citations and explanations (Rule 70.7):

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

Reference is made to the following documents:

D1: US-A-5 739 193 (WALPITA ET AL) 14 April 1998 (1998-04-14)

D2: US 2002/158305 A1 (DALMIA SIDHARTH ET AL) 31 October 2002 (2002-10-31)

D3: US 2004/034489 A1 (OGINO TATSUYA ET AL) 19 February 2004 (2004-02-19)

1. The present application relates to modules for wireless application, and in particular, to a signal processing module, a diplexer and a balun, the modules comprising components integrated in laminate layers.

2. Document D1 discloses (col. 6, l. 37 - col. 7, l. 49) a signal processing module suitable for wireless applications comprising:

a liquid crystalline polymer (LCP) layer having a first surface and a second surface opposite the first surface;

a first patterned metal layer on the first surface of the LCP layer;

a second patterned metal layer on the second surface of the LCP layer, wherein the first and second metal layers are patterned to form integrated components.

Document D1 further discloses that the metal clad LCP layer is stacked and interconnected to other dielectric laminates so that a multilayer substrate for a module is formed.

Thus, the subject matter of claim 1 appears to differ from this known module at least in that

(i) the first and second metal layers interact with one another to form a first resonator and a second resonator; and

(ii) the LCP layer is unfilled.

The subject matter of claim 1 seems, therefore, novel (Article 33(2) PCT).

Document D1 discloses modules for application in antennas, filters and other RF and microwave elements. Therefore, the integration of resonators as proposed in claim 1 , i.e. feature (i) cannot be seen as involving an inventive step.

However, document D1 does not disclose the use of unfilled LCP layers. Moreover,

this document (see col. 3, l. 4 - 47) teaches away from the use of unfilled polymers.

None of the other cited documents suggests to provide a layer of unfilled liquid crystalline polymer in a module for wireless applications.

In view of the available prior art, the subject matter of claim 1 appears, therefore, to involve an inventive step (Article 33(3) PCT).

3. The same reasoning applies, mutatis mutandis, to the subject matter of independent claims 10 and 21 which are directed, respectively, to a diplexer and a signal processing module comprising an unfilled LCP layer. Said claims appear, therefore, also to meet the requirements for novelty and inventive step.

4. Independent claim 16 is directed to a balun for wireless application. Its subject matter is distinguished from the module known from document D1 at least in that it comprises

an unfilled first outer organic layer and an unfilled second outer organic layer.

Since none of the available prior art documents discloses such layers, the subject matter of claim 16 seems to involve an inventive step for similar reasons as that of claims 1, 10 and 21.

5. Dependent claims 2 - 9, 11 - 15, 17 - 20 and 22 - 24 which define preferred embodiments of the invention are dependent on claims 1, 10, 16 and 21, respectively, and as such also appear to meet the requirements of the PCT in respect of novelty and inventive step.

<u>Re Item VIII</u>

Certain observations on the international application

1. The description (page 10, lines 22 - 25; page 12, line 18) implies that the subject matter for which protection is sought may be different to that defined by the claims. This results in lack of clarity of the claims (Article 6 PCT) when the description is used to interpret them (see the Guidelines, paragraph 5.30).

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reduction on the order of λ/40, 3) low insertion loss comparable to ceramic monoblock filters for comparable size, bandwidth and attenuation specifications, 4) a high reliability demonstrable by extensive life testing, 5) minimal temperature dependence performance variation, 6) fewer metal layers to achieve the same density as LTCC, 7) a single substrate that may be used at multiple frequencies (1GHz-100GHz) to implement different functions such as filters, diplexers and baluns, 8) conducive for large area (12x18 square inch or approximately 30.5x45.7 square centimeter) processing, 9) faster time to market due to lesser number of layers, 10) excellent hermetic properties (e.g., 0.04% moisture absorption) comparable to ceramics, and 11) eliminates several levels of packaging such as integrated circuit (IC) and discretes on LTCC on PCB on PCB, or TFOS and IC on PCB on PCB, or LTCC on PCB and other variants to ultimately multiple ICs on single PCB or multilayer polymer substrate.

Bandpass Filter Design

[00117] Radio frequency (RF) filters are generally used to remove the out-of-band energy and perform rejection of image-band signals. The design of RF filters in most architectures is becoming a problem since center frequencies are scaling towards the multi-gigahertz range for most RF standards. As the carrier frequency becomes higher, the loaded Q (carrier frequency / 3dB bandwidth) for filters becomes higher, which places higher demand on the unloaded quality factor for components such as inductors, capacitors and resonators that make up the filter device. These filters and signal processing units can meet the specifications of cavity filters, MLC and LTCC filters and signal processing devices with equivalent or better performance in smaller or similar footprints. In particular, the present invention comprises a multilayer organic substrate that utilizes thin dielectric layers such as liquid crystalline polymer films that are either filled with high k dielectric constant particles or unfilled, and interconnected in a configuration that allows for blind and buried via structures to support the integration of multiple RF components such as filters, baluns, diplexers, and a combination thereof within the substrate for different communication standards such as 802.11a/b/g, local multipoint distribution service (LMDS)/multichannel

provide lower transmission zeroes. These resonator arms can be connected using capacitive coupling or inductive coupling between the resonators. The Cinter-resonator 806 conceptually represents reactance present in the form of capacitance, inductance, and mutual inductance between adjacent resonators or non-adjacent resonators which help in attaining more degrees of freedom based on control theory for the addition of transmission zeroes, control of bandwidth, and control of center frequency.

[00119] In addition, with respect to FIG. 14A, lowpass filter elements are provided at the input and output, such as the inductors Llowpass 808 and capacitors Clowpass 810, to achieve high attenuation at the second harmonic and third harmonic of the center frequency. In addition, the capacitors Cmatch1 820 are provided to match impedances between sections. For simplicity, however, no parasitic components have been shown in Fig. 14A.

[00120] As an example, a two pole filter constructed in accordance with the present invention using two metal layers on two sides of a thin laminate substrate and then shielded on both sides has a footprint of 3x3mm, a height of 1.5mm and emulates the performance of a 4x5mm monoblock filter having a height of 1.8mm. Using processing techniques in accordance with the invention on a 12"x12" (or approximately 30.5cm x 30.5cm) substrate, it is possible to fabricate approximately 6500 such components with filter-to-filter spacing included, which illustrates its cost effectiveness. A filter according to the present invention requires just two metal layer pattering because of the CPW-type topology compared to the multi-layers in ceramic filters or molded cavity filters. This also reduces design time and processing time as compared to ceramic filters or molded cavity filters. Such a design is discussed in U.S. Publication No. 20040000701A1, published January 1, 2004, entitled "Stand-Alone Organic-Based Passive Devices," and assigned to the owners of the present application.

electromagnetic wave at a particular frequency (f). Such reduction in size is available for all passive signal distribution devices where f is typically the center frequency of balun, coupler, filter or the 3dB transmission points of low pass filter, high pass filters, diplexers, and multiplexers. Using known processing techniques on a 9"x12" (22.9cm x 30.5cm), 12"x12" (30.5cm x 30.5cm), 18"x12" (45.7cm x 30.5cm), 20"x24" (50.8cm x 61cm), 40"x48" (101.6cm x 121.9cm) and similar large area substrate, it is possible to fabricate approximately thousands of such components with component-to-component spacing included, which illustrates its cost effectiveness and cost reduction. The spacing and design rules used for the substrates, components and between components includes both the tooling for dicing, encapsulation, wirebondability, direct chip attach such as flip chip, and lastly also includes pads and openings for RF testability. A component or combination of components according to the present invention requires a minimum of two metal, three or four metal layers pattering because of the CPW, microstrip, stripline type topologies respectively compared to the multi-layers in ceramic, molded cavity, LTCC components. It thus becomes possible to eliminate the need for multiple levels of packaging from a performance and size standpoint and have ultimately this particular solution as the final or the only PCB required for communication devices. This also reduces design time and processing time as compared to ceramic filters or molded cavity filters.

Multiple Components Design

[00156] While the filters, diplexers, multiplexers, and baluns above have each been described separately, one of ordinary skill in the art would recognize that other embodiments in accordance with the present invention could contain one or more of the filters, diplexers, multiplexers, and baluns. For example, a fabricated device in accordance with the present invention could contain at least one filter, at least one diplexer, and at least one balun. In order to include filters, diplexers, multiplexers, and baluns or other components in the same device while keeping the size of the device small, an embodiment of the presention may place high performance and low performance components on particular layers and further, high K dielectric particles may be incorporated into certain layers of the device.

[0006A] It is typical for LTCC front-end modules to comprise more than 10-15 metal metallic layers with microvias connecting each layer, and in many instances also include SAW and FBAR filters mounted on the multiple ceramic layers to meet the more stringent requirements of bandpass filters. The need for many layers to provide the needed density translates to more design time and higher tooling cost and problems of shrinkage and performance issues. In addition, increases in density have been slow, and has not reached further than 75 components / cm^2. To meet current density requirements, discrete components are mounted on the top surface of LTCC modules as discrete components. Besides the need for discretes to achieve the desired density or using thin film based devices, such modules have to be mounted on a printed circuit board (PCB). Further, LTCC also generally suffers from higher costs since it generally cannot be manufactured in panel sizes larger than 6x6 square inches (or approximately 15.2x15.2 square centimeters). Moreover, LTCC generally has relatively low performance due to process tolerances and relatively high dielectric losses (e.g., tan δ =0.005-0.007 at 1GHz).

[0006B] In addition, U.S. Patent No. 5,739,193 to Walpita et al. discloses a polymeric composition having a high dielectric constant which varies little with temperature and that is made from a thermoplastic polymer, a high dielectric ceramic having a dielectric constant of at least about 50 at 1.0 Ghz and 20 degrees C., and a second ceramic material having a dielectric constant of at least about 5.0 at 1.0 GHz and 20 degrees C., where the high dielectric ceramic and the second ceramic material have temperature coefficients that are opposite in sign from one another. U.S. Patent Publication No. 2002/0158305A1 to Dalmia et al. discloses a substrate adapted for use in integrated circuits, a method for fabricating the substrate, and a computer program embodied in a computer-readable medium for optimizing the design of an integrated inductor in the substrate. The substrate includes a substrate layer of organic material, a conductor layer fabricated on an upper surface of the substrate layer, and an integrated inductor fabricated on an upper surface of the conductive layer. U.S. Patent Publication No. 2004/0034489A1 to Ogino et al. discloses a high frequency module board device having a high frequency transmitting and receiving circuit for modulating and demodulating a high frequency signal.

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[0007] Thus, there is an unsatisfied need in the industry for a high frequency, low loss, inexpensive filters, baluns, and diplexers having a relatively small footprint for multi-band, multi standard applications.

SUMMARY OF THE INVENTION

[0008] In accordance with an embodiment of the present invention, a signal processing module for wireless applications includes a Liquid Crystalline Polymer (LCP) layer having a first surface and a second surface opposite the first surface, a first patterned metal layer on the first surface of the LCP layer, a second metal patterned metal layer on the second surface of the LCP layer, where the first and second metal layers are patterned to form integrated components such that the first and second metal layers interact with one another to form a first resonator and a second resonator, a first prepreg layer on the first metal layer opposite the LCP layer and a second prepreg layer on the second metal layer opposite the LCP layer, and a first laminate

number of components required to achieve a filtering function by removing the need for capacitors of the resonators. However, a disadvantage is the increase in length of the metallization to increase the capacitance, though the increased inductance could increase loss in the circuit. If the inductor element becomes too large or too lossy, then it may be desirable to use an alternative circuit design, such as that illustrated in FIG. 1A. It should be noted that in the circuits of FIG. 1A and FIG. 1B, the coupling between the components can be achieved by magnetic coupling, electric coupling or a combination thereof.

[0057] Illustrative physical layouts of dielectric filters in accordance with the equivalent circuit diagram of FIG. 1A are depicted in FIGS. 2-4. The dielectric filters of FIGS. 2-4 have a two-pole structure and an additional pole attained by the mutual inductance and the capacitor 24 according to the equivalent circuit diagram shown in FIG. 1A.

[0058] With general reference to FIGS. 2A-2C, illustrated is a surface mounted device (SMD) embodiment of the filter illustrated by the circuit of FIG. 1A. Specifically, the organic bandpass filter 200 comprises inductors 212 and 214, which are meandering inductors formed close to each other on an organic dielectric layer 236 (which can be a thin laminate such as LCP or PPE, but is not limited to these) and is preferably configured as either a shorted hybrid CPW-stripline (where lines that form meandering inductors 212 and 214 are connected to a coplanar ground, that is, in-built shielding 230), or a stripline in the presence of coplanar in-built shielding 230 and additional grounds 248 and 250 that are connected to the plated through holes 232 and/or external shield electrodes 234.

[0059] Since these inductors are very close to each other, the magnetic coupling between these filters, represented by M in FIG. 1A, can increase the pass bandwidth of the filter, thereby decreasing its performance. However, an inter-

[00121] In an exemplary embodiment, a bandpass type filter 900 in FIG. 15 was designed for WLAN (802.11 b/g) type applications and can also be used for Bluetooth, and other ISM band type applications. The bandpass type filter 900 intended for 2.4 GHz WLAN front-end RF filter type applications was designed using the following lumped element components illustrated in FIG. 14A: LRES1 816 =LRES2 818 = 5.1nH, CRES1 812 =CRES2 814 = 0.9pF, Lmutual 804 =26nH, Cmutual 802 =0.088pF, Cmatch1 820 = 0.3pF, Clowpass 810 = 0.52, Llowpass 808 = 0.35nH, and Cinter-resonator 806 = 0.05pF. In this instance CRES1 812, CRES2 814 exist as the parasitics of the inductors LRES1 816 and LRES2 818 and shunt capacitance of Cmatch1 820 and Cmatch2 822. As illustrated in FIG. 16, the filter depicts a 1dB passband of 100MHz with insertion loss less than 1.3dB from 2.4-2.5GHz and transmission zeroes at 2.8GHz and 1.6GHz. Referring to FIG. 15, this filter is constructed using one layer of LCP that is 2 mils thick and metal layers M1 904 and M2 906 on either side. In addition, the internal metal layers M1 904, M2 906, and M3 908 and the top and bottom shielding layers 902, 910 may contain vias 912, which are denoted herein and throughout the application by the small triangles arranged in a circular pattern. It is packaged with 4 mil prepreg (e.g., Rogers 4450B) on either side (refer above and to U.S. Publication No. 20040000701A1, which is referenced above, for variations) followed by 8 mil hydrocarbons (e.g., Rogers 4003, 4350 type) on either side. This stack up conforms to the one shown in FIG. 17A and discussed herein.

[00122] Specifically, FIG. 17A discloses six metal layers 1701-1706, as denoted by the dark lines. Both the top 1701 and bottom 1706 metal layers may function as ground shields. The metal layers 1703, 1704 on each surface of the LCP layer 1710 may contain inductors and parallel plate capacitors. The metal layers 1702, 1705 on the laminate layers 1707, 1708 (e.g., Rogers 4350B laminate) adjacent the prepreg layers 1709 (e.g., Rogers 4450 prepreg) are optional and may contain additional components if desired, such as for added density. In accordance with an embodiment of the present invention, the inductors are preferably formed on the LCP layer 1710 and the capacitors are formed on either the LCP layer 1710 or the laminate layers 1707, 1708. FIG. 17B is an extension of FIG. 17A, in which an additional LCP layer 1712 with metal layers on opposite sides thereof has been added. More components, including parallel plate capacitors and inductors can be

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placed on this additional LCP layer 1712. This additional LCP layer 1712 is separated from the other LCP layer 1710 by an additional prepreg layer 1709, though the layers may be electrically connected by microvias 1714.

[00123] FIG. 17C illustrates the layers shown in FIG. 17B, except that high K layers 1716, 1718 have been substituted as for the laminate layers 1707, 1708. When compared to the laminate layers 1707, 1708, the high K layers 1716, 1718 increase the separation and increase the capacitance for capacitor components that may be placed on the high K layers 1716, 1718. Generally, the non-critical, lower-performing components would be placed on the high K layers 1716, 1718. FIG. 17D illustrates three LCP layers 1720, 1712, 1710 that are separated by two prepreg layers 1709 (e.g., Rogers 4450B prepreg). An aspect of the stackup shown in FIG. 17D compared to the previous stickups in FIGS. 17A-C is that this is an extremely thin stackup which may be on the order of a 0.3mm thick substrate. Four metal layers are shown in FIG. 17D, which may contain components such as capacitors and inductors, providing for excellent density. FIG. 17D may be known as a high performance substrate. One of ordinary skill would recognize that the stackup in FIG. 17D is not limited to 3 LCP layers 1720, 1712, 1710, but could contain additional layers, including another LCP layer that is separated from the other LCP layer by a prepreg layer.

[00124] FIG. 17E illustrates an inner high K layer 1730 that is positioned between two laminate, LCP, or high K layers 1732, 1734. In particular, the high K layer 1730 is separated from each laminate (e.g., Rogers 4350B laminate), LCP, or high K layer 1732, 1734 by prepreg layers 1709 on opposite sides of the high K layer 1730. The high K layer 1730 and each of the laminate, LCP, or high K layers 1732, 1734 may contain metal layers on each surface to provide for integrated components such as inductor and capacitors. The stackup shown in FIG. 17E may be suitable for a baluns which may have a more relaxed performance specification. In such a case, the high K middle layer 1730 does not have to be fabricated with such stringent requirements (e.g., thickness), and is appropriate for use as an inner layer. FIG. 17F discloses a stackup similar to that shown in FIG. 17A, with the addition of exterior RCF (resin coated foil) layers 1740, 1742. RCF (resin coated foil) allows for the same densities for lines and

spacing and microvias but at a lower cost compared to high K and LCP. In addition, in FIG. 17F, the laminate layers 1732, 1734 could also be substituted with high K or LCP layers.

[00125] When working with hybrid CPW-stripline topology, the higher performance components will typically need to be further away from ground while the lower performance components may be closer to ground. For example, in FIG. 17B, inductors may be placed in the inner LCP layers while parallel plate capacitors may be placed on the laminate layers. However, parallel plate capacitors could also be placed on the inner LCP layers as well.

[00126] Referring back to FIG. 15, this topology uses the distance between the coils of the inductors to control the Cmutual 802 and Lmutual 804 to control the bandwidth and the fundamental transmission zero on the lower side or higher side of the center frequency. The Cinter-resonator 806 can be added as inter-digital or a parallel plate capacitor. Other degrees of freedom are the LCP or internal polymer thickness. For example the same inductor on 1 mil LCP gives a LRES1 816 =LRES2 816 =10nH, but with a parallel CRES1 812 = CRES2 814 = 0.12pF. The Cmatch1 820/Cmatch2 822 on either side controls the desired impedance of the filter. Such a topology can be used as a one pole or multiple pole filter with topologies shown in FIG. 14A or variations shown in FIGS. 14B-14D. Another possible variation for this design is to use the stackup in FIG. 17B with two LCP layers. As seen from internal layers M2 906 and M3 908 in FIG. 15, there are limitations to the ways of laying inductors next to each other. This becomes a limitation for the different kinds of filters. In this scenario, inductors can be split up between four metal layers which are adjacent to the LCP layers shown in FIG. 17B. The inductors now can be vertically above each other or offset from each other in X, Y, and Z dimensions which gives designers more freedom for design parameters such as BW, and transmission zeroes. Finally, another mechanism for optimal size reduction is to place the capacitors CMatch1 820, CMatch2 822 and CRES1 812, CRES2 814, essentially all capacitors on LCP layers away from the central LCP layers which preferably includes only of inductors. FIGS. 17C and 17D can now be used for such a design. The outer LCP

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cores (i.e., the laminate layers) or the high K layers have to be now further away from the innermost layer containing the high current carrying inductors. In such a case, thicker prepreg layers should be used to maintain the required distance (for isolation) of the inductors from the grounds.

[00127] In comparison to this design, design examples shown in US Publication No. 20040000701A1, which is referenced above, show a possible generic design, which does not use significant parasitics of components. Such designs are useful at higher frequencies where component values become smaller and parasitics become difficult to control or at lower frequencies in applications such as basestations, LMDS, MMDS and access points where space is not critical but performance and integration are.

[00128] FIG. 18 shows an illustrative embodiment of a wider bandwidth filter 1800 applicable for application as a bandpass filter that passes 4.9-5.9 GHz with low insertion loss and attenuation of 2nd and 3rd harmonics of the pass band (9.8-11.8GHz, 14.7-18GHz) and also attenuates 802.11b/g frequencies and cellular frequencies below 2.2 GHz. This stack up conforms to the one shown in FIG. 17A. However, 1 mil LCP is used with 4 mils of Rogers 4350 laminate and Rogers 4450 prepreg on either side. Similar design principles presented for the previous circuit in FIG. 15 are also applicable for this particular circuit shown in FIG. 18. The size of the above mentioned circuits are roughly 2mmx2mm and integrate nine components at 2400 MHz and seven components at 5500 MHz, which equates to a component density upwards of 150-200 components /cm2. The other design suggestions may increase this count to upwards of 500-1000components/cm2.

[00129] The use of high K layers will now be discussed in more detail. An LCP layer or other laminate layer can be filled with high K dielectric particles or incorporate a high K deposited thin film. Incorporation of the high K particles may be achieved by introducing a surfactant onto high k particles, such as Barium titinate,

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[00135] According to an embodiment of the present invention, the equivalent circuit as illustrated in FIG. 19 was designed using similar layers and cross-section used for design of the bandpass filters previously discussed. In particular, the entire circuit was designed using four metal layers, which includes two metal layers 1212, 1214 for the top and bottom shields and two inner metal layers 1203, 1205 for the inductors and capacitors cross-section used for design of the bandpass filters discussed earlier. Figure 20 shows one possible layout for the resultant structure which achieves the desired specifications. The solid lines shown in FIG. 20 show the metal pattern on one of the inner layers and the dotted lines show the metal patterning on the corresponding layer either above or below. The capacitors 1012-1052 and inductors 1002-1050 in FIG. 20 correspond to the similarly labeled capacitors and inductors in FIG. 19. The top and bottom stripline grounds 1212, 1214 are each approximately 1mm away from the inner layers. Using low loss (er=2.9, tan d=0.002 below 10GHz, and tan d=0.003 below 100 GHz) 2 mil thick LCP 1202 for embedded parallel plate capacitors or inter-digital capacitors helps achieve unloaded Q>200 for capacitances in the range of 0.1-5pF for frequencies >2GHz with capacitance densities on the order of 2pF/mm2. The resultant size for the finished component was approximately 20mm x 5mm x 2mm. This can be compared to common ceramic monoblock diplexers used for such applications are on the order of 35mm x 12mm x 5mm. The measured data for such a diplexer is shown in FIG. 21. The insertion loss within the passband is <3dB, and the attenuation of the respective bands meets the specifications listed earlier.

[00136] FIG. 22 shows another illustrative implementation of a layout the high performance diplexer in FIG. 19. The layout in FIG. 22 embeds the functionality of 35 components and is used for the separation of IF bands of the down converted frequency in satellite TV link. The performance of this device controls the clarity and resolution of channels to the TV units that the satellite TV feeds. The inner layers are shown as 1202 and 1204 in Figure 22. The number of components can be reduced significantly for devices which may not require as high a performance as the one shown.

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1. A signal processing module for wireless applications, comprising:

an unfilled Liquid Crystalline Polymer (LCP) layer (1710) having a first surface and a second surface opposite the first surface;

a first patterned metal layer (904, 1202, or 1703) on the first surface of the LCP layer (1710);

a second patterned metal layer (906, 1204, or 1704) on the second surface of the LCP layer (1710), wherein the first (904, 1202, or 1703) and second metal layers (906, 1204, or 1704) are patterned to form integrated components such that the first (904, 1202, or 1704) and second metal layers (906, 1204, or 1704) interact with one another to form a first resonator and a second resonator;

a first prepreg layer (1709) on the first metal layer (904, 1202, or 1703) opposite the LCP layer (1710) and a second prepreg layer (1709) on the second metal layer (906, 1204, or 1704) opposite the LCP layer (1710); and

a first laminate layer (1707) on the first prepreg layer (1709) opposite the first metal layer (904, 1202, or 1703), and a second laminate layer (1708) on the second prepreg layer (1709) opposite the second metal layer (906, 1204, or 1704).

2. The module of Claim 1, wherein the first resonator comprises a first inductor (816 or 818) formed in the first patterned metal layer (904, 1202, or 1703) and a second inductor (816 or 818) formed in the second patterned metal layer (906, 1204, or 1704), wherein the first inductor (816 or 818) is connected by a first microvia (912) to the second inductor (816 or 818).

3. The module of Claim 1, wherein the first resonator (816 or 818) is magnetically coupled to the second resonator (816 or 818).

4. The module of Claim 1, further comprising a third resonator formed in the first (904, 1202, or 1703) and second metal layers (906, 1204, or 1704) and electrically connecting the first resonator (816 or 818) to the second resonator (816 or 818), wherein the third resonator provides a primary attenuation zero in a stopband.

5. The module of Claim 1, wherein the first (816 or 818) and second resonators (816 or 818) comprise transmission line resonators.

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6. The module of Claim 1, wherein the first (816 or 818) and second resonators (816 or 818) comprise one or more of co-planar waveguide, stripline, and microstrip topologies.

7. The module of Claim 1, further comprising a third metal layer (1701) on a first surface of the first laminate layer (1707) and patterned to form a first capacitor plate, and a fourth metal layer (1702) on a second surface of the first laminate layer (1707) opposite the first surface and patterned to form a second capacitor plate, wherein the first capacitor plate and second capacitor plate form a parallel plate capacitor.

8. The module of Claim 1, further comprising a first shielding layer (902) on the first laminate layer (1707) opposite the first prepreg layer (1709) and a second shielding layer (910) on the second laminate layer (1706) opposite the second prepreg layer (1709).

9. The module of Claim 1, wherein the integrated components include at least one of capacitors (806, 810, 820, or 822)and inductors (816 or 818).

10. A diplexer (1100) for a multi-band wireless application, comprising:

an unfilled Liquid Crystalline Polymer (LCP) layer (1202) having a first surface and a second surface opposite the first surface;

a first patterned metal layer (1203) on the first surface of the LCP layer (1202);

a second patterned metal layer (1205) on the second surface of the LCP layer (1202), wherein the first (1203) and second metal layers (1205) are patterned to form integrated components such that the first (1203) and second metal layers (1205) interact with one another to form a first filter and a second filter connected by a common port;

a first prepreg layer (1204) on the first metal layer (1203) opposite the LCP layer (1202), and a second prepreg layer (1206) on the second metal layer (1205) opposite the LCP layer (1202); and

a first laminate layer (1208) on the first prepreg layer (1204) opposite the first

metal layer (1203), and a second laminate layer (1210) on the second prepreg layer (1206) opposite the second metal layer (1205).

11. The diplexer (1100) of Claim 10, wherein the first filter comprises a first inductor formed in the first patterned metal layer (1203) and a second inductor formed in the second patterned metal layer (1205), wherein the first inductor is connected by a first microvia to the second inductor.

12. The diplexer (1100) of Claim 10, wherein the first (1203) and second metal layers (1205) comprise one or more of co-planar waveguide, stripline, and microstrip topologies.

13. The diplexer (1100) of Claim 10, further comprising a third metal layer on a first surface of the first laminate layer (1208) and patterned to form a first capacitor plate, and a fourth metal layer on a second surface of the first laminate layer (1208) opposite the first surface and patterned to form a second capacitor plate, wherein the first capacitor plate and second capacitor plate form a parallel plate capacitor.

14. The diplexer (1100) of Claim 10, further comprising a first shielding layer (1212) on the first laminate layer (1208) opposite the first prepreg layer (1204) and a second shielding layer (1214) on the second laminate layer (1210) opposite the second prepreg layer (1206).

15. The diplexer (1100) of Claim 10, wherein the integrated components include at least one of capacitors and inductors.

16. A balun for a wireless application, comprising:

a high K organic layer (1730) having a first surface and a second surface opposite the first surface;

a first patterned metal layer on the first surface of the high K organic layer (1730);

a second metal patterned metal layer on the second surface of the high K

organic layer (1730), wherein the first and second metal layers are patterned to form integrated components such that the first and second metal layers interact with one another to form a first passive device and a second passive device;

a first prepreg layer (1709) on the first metal layer opposite the high K organic layer (1730), and a second prepreg layer (1709) on the second metal layer opposite the high K organic layer (1730); and

an unfilled first outer organic layer (1732) on the first prepreg layer (1709) opposite the first metal layer, and an unfilled second outer organic layer (1734) on the second prepreg layer (1709) opposite the second metal layer.

17. The balun of Claim 16, wherein the first outer organic layer (1732) comprises one of a laminate layer and LCP layer.

18. The balun of Claim 16, wherein the first metal layer is patterned to form a first capacitor plate and the second metal layer is patterned to form a second capacitor plate, and further comprising a third metal layer on the first outer organic layer (1732) patterned to form a third capacitor plate, and wherein the first, second and third capacitor plates form a capacitor.

19. The balun of Claim 16, wherein the integrated components include at least one of capacitors and inductors.

20. The balun of Claim 16, further comprising a first shielding layer on the first outer organic layer (1732) opposite the first prepreg layer (1709) and a second shielding layer on the second outer organic layer (1734) opposite the second prepreg layer (1709).

21. A signal processing module for multi-band wireless applications, comprising:

an unfilled first Liquid Crystalline Polymer (LCP) layer (1710) having a first surface and a second surface opposite the first surface;

a first patterned metal layer on the first surface of the first LCP layer (1710);

a second patterned metal layer on the second surface of the first LCP layer

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(1710), wherein the first and second metal layers are patterned to form integrated components such that the first and second metal layers interact with one another to form at least a first filter and a second filter connected by a common port;

an unfilled second LCP layer (1712) having a first surface and a second surface opposite the first surface;

a third patterned metal layer on the first surface of the second LCP layer (1712);

a fourth patterned metal layer on the second surface of the second LCP layer (1712), wherein the third and fourth metal layers are patterned to form integrated components such that the third and fourth metal layers interact with one another to form at least a first filter and a second filter connected by a common port;

a first prepreg layer (1709) disposed between the first (1710) and second LCP layers (1712);

a second prepreg layer (1709) on the second metal layer opposite the first LCP layer (1710), and a third prepreg layer (1709) on the third metal layer opposite the second LCP layer (1712); and

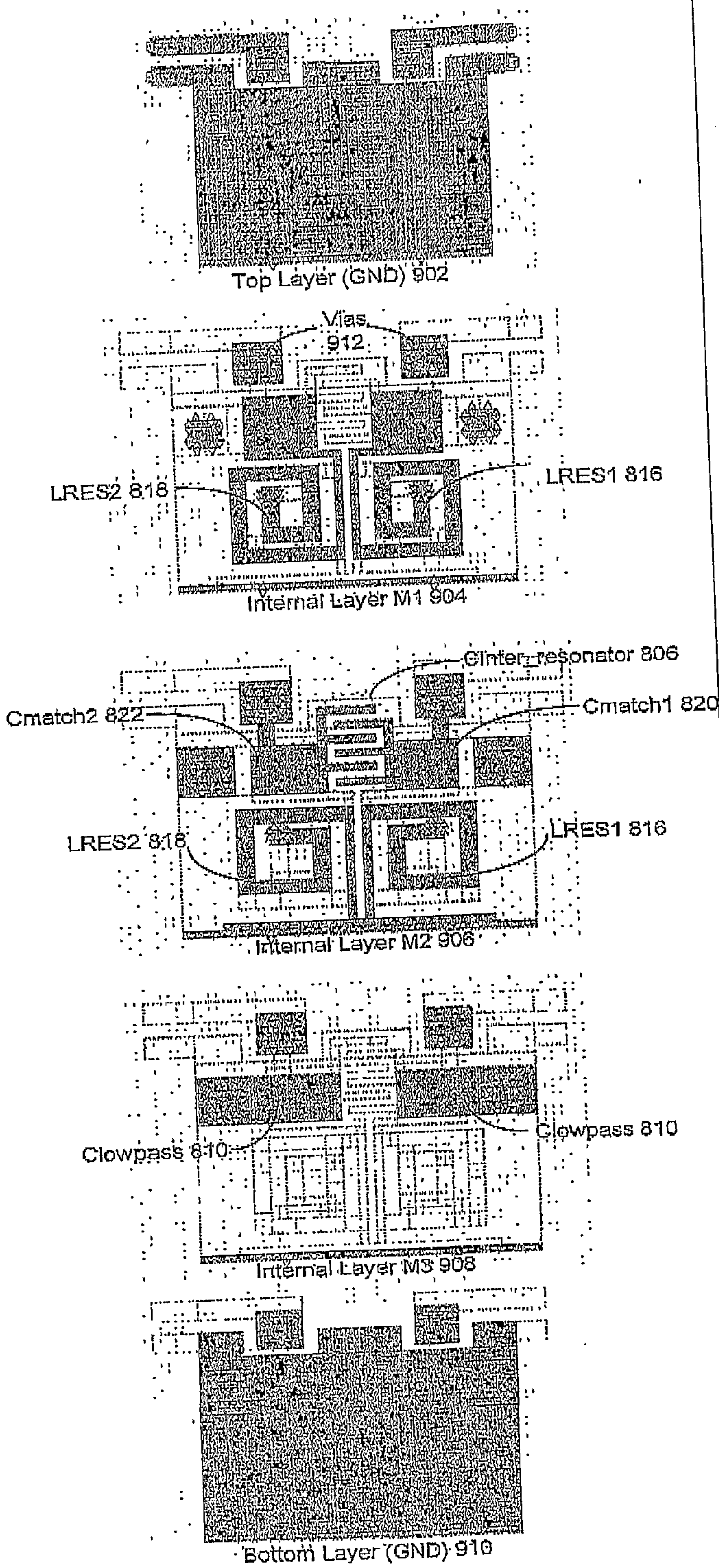
a first outer organic layer (1707, 1732) on the second prepreg layer opposite the second metal layer, and a second outer organic layer (1708, 1734) on the third prepreg layer (1709) opposite the third metal layer.

22. The module of Claim 21, further comprising a first shielding layer on the first outer organic layer (1707, 1732) opposite the second prepreg layer (1709) and a second shielding layer on the second outer organic layer (1708, 1734) opposite the third prepreg layer (1709).

23. The module of Claim 21, wherein the first outer organic layer (1707, 1732) comprises one of a laminate layer, LCP layer or high K organic layer.

24. The module of Claim 21, further comprising a first resin coated foil (RCF) layer (1740) on first outer organic layer (1707, 1732)) opposite the second prepreg layer (1709); and

a second RCF layer (1742) on the second outer organic layer (1708, 1734)) opposite the third prepreg layer (1709).



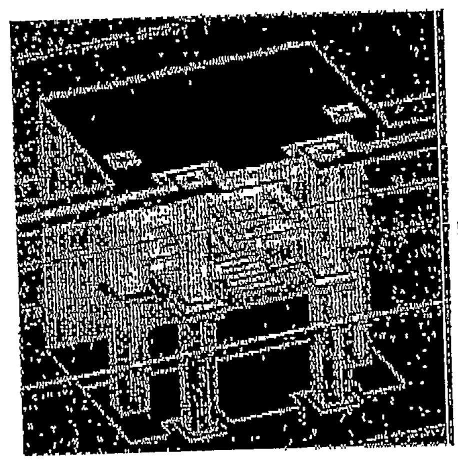


FIG. 15

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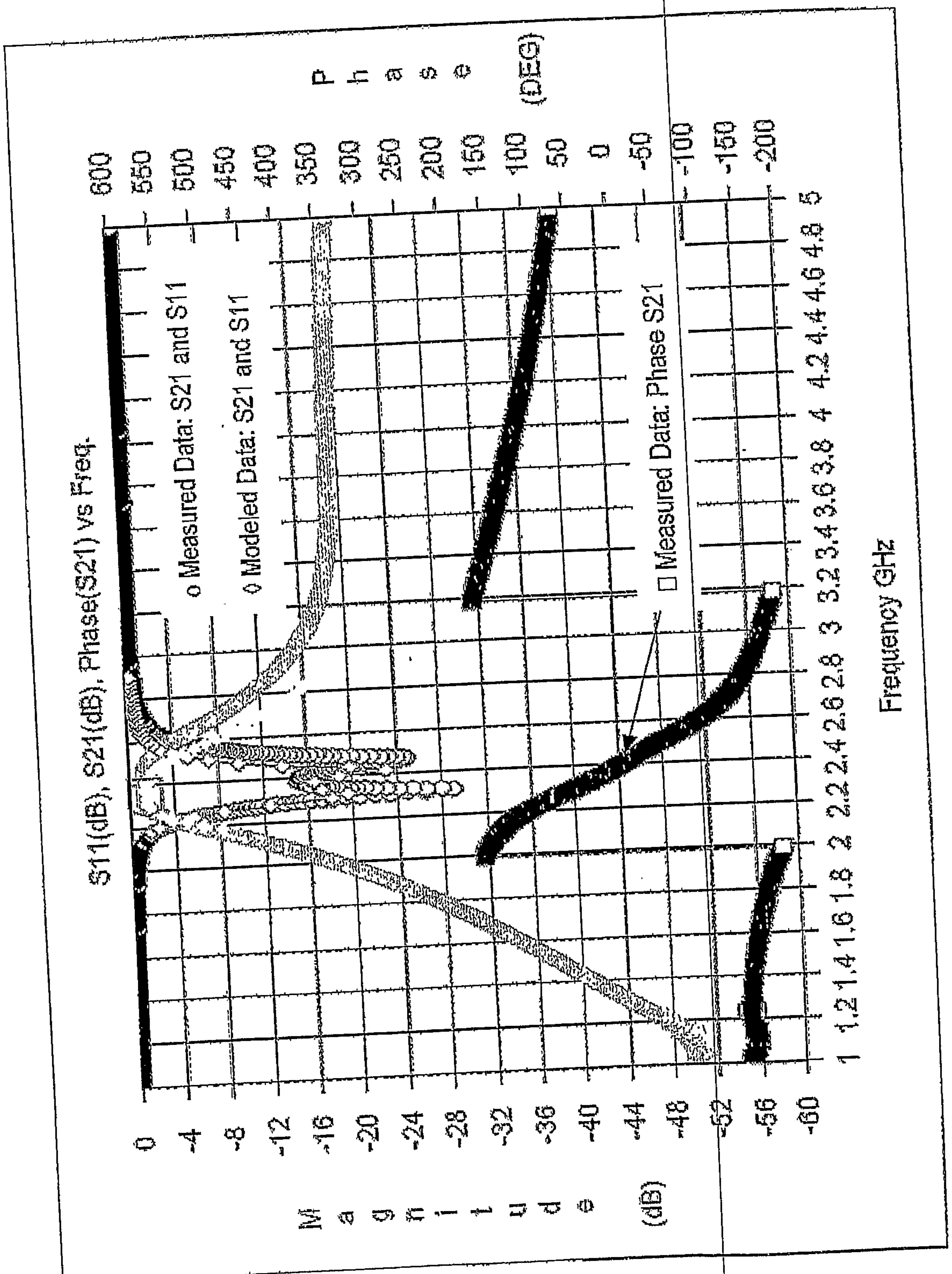

FIG. 16

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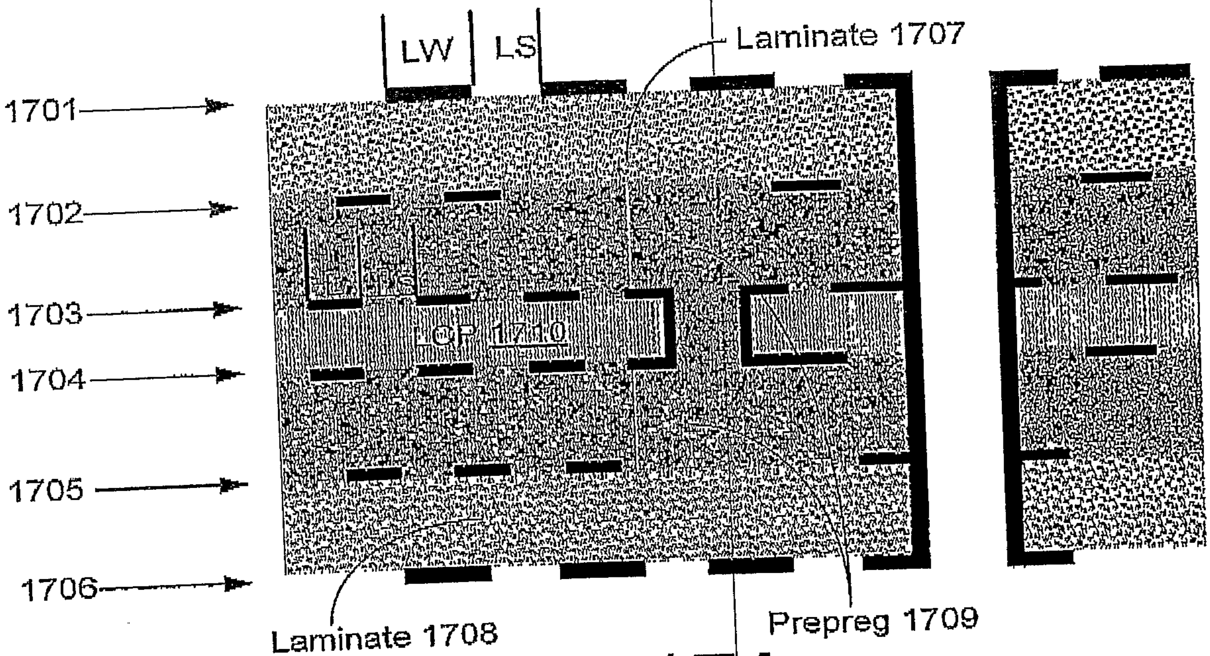

FIG. 17A

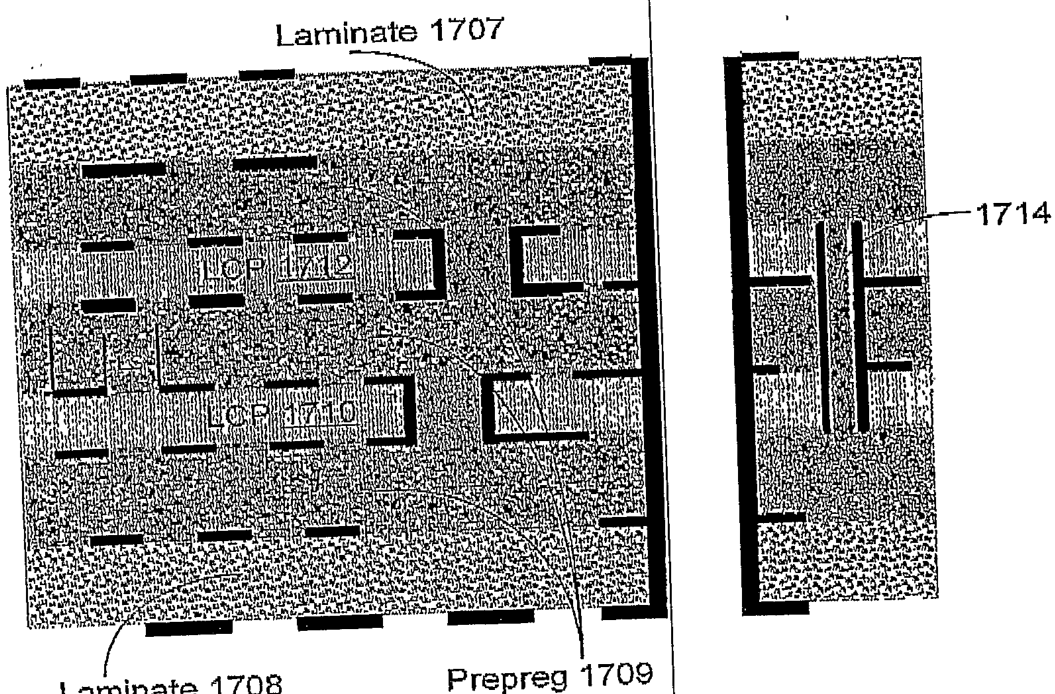

FIG. 17B

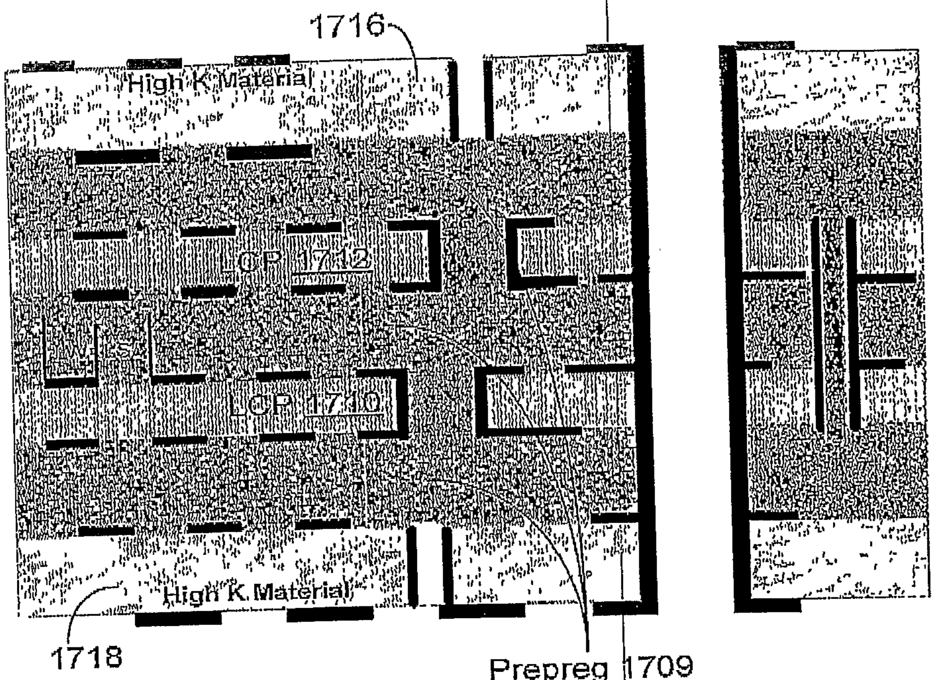

FIG. 17C

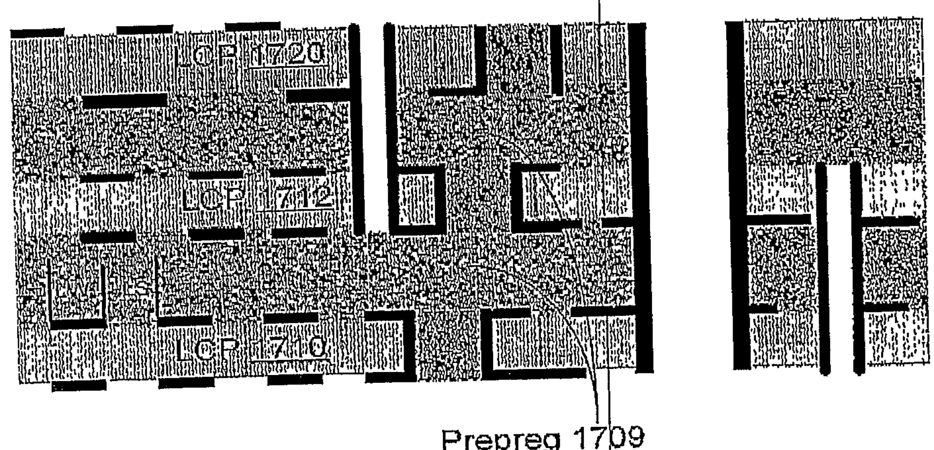

FIG. 17D

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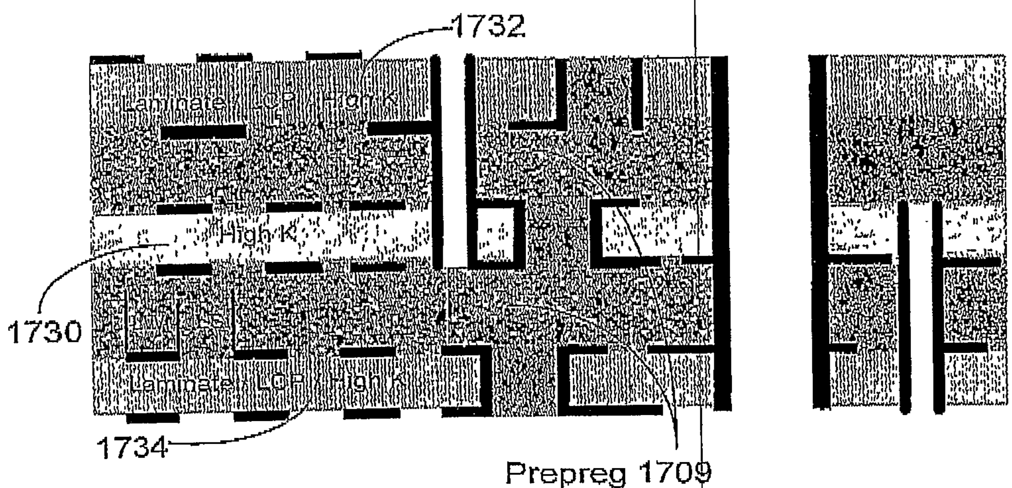

FIG. 17E

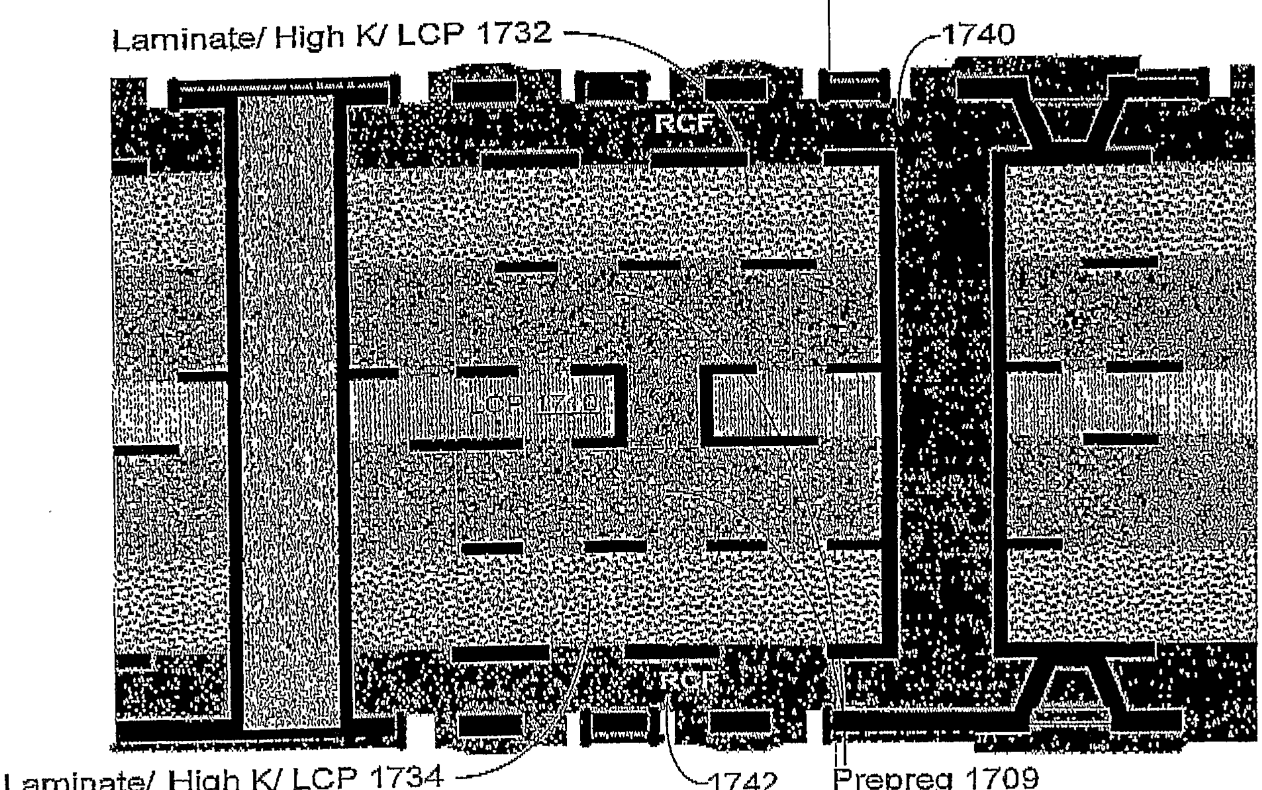

FIG. 17F

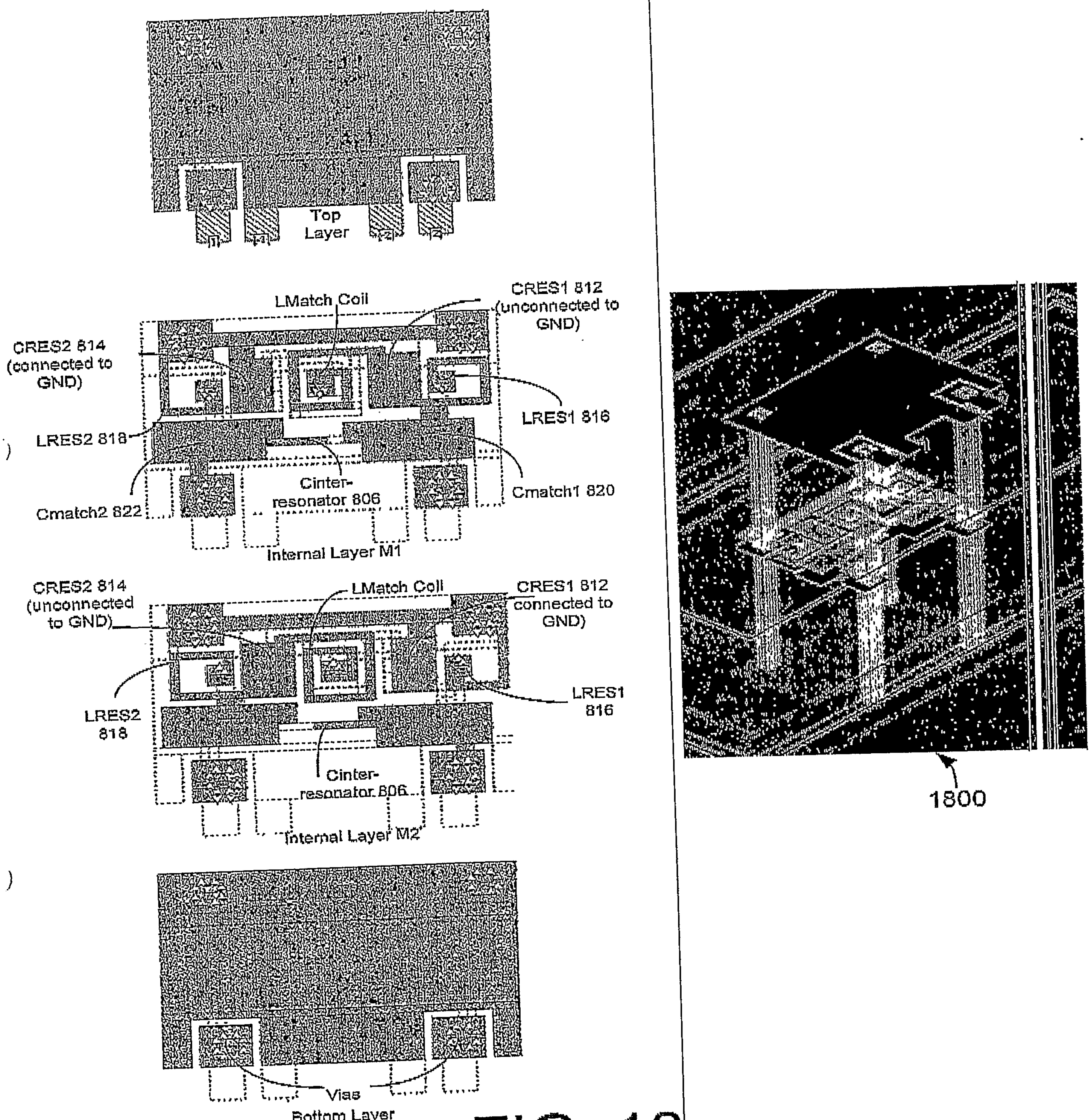
Top
Layer
LMatch Coil
CRES1 812
(unconnected to
GND)
CRES2 814
(connected to
GND)
LRES1 816
LRES2 818
Cinter-
resonator 806
Cmatch1 820
Cmatch2 822
Internal Layer M1
CRES2 814
(unconnected
to GND)
LMatch Coil
CRES1 812
connected to
GND)
LRES1
816
LRES2
818
Cinter-
resonator 806
Internal Layer M2
Vias
Bottom Layer
1800

FIG. 18

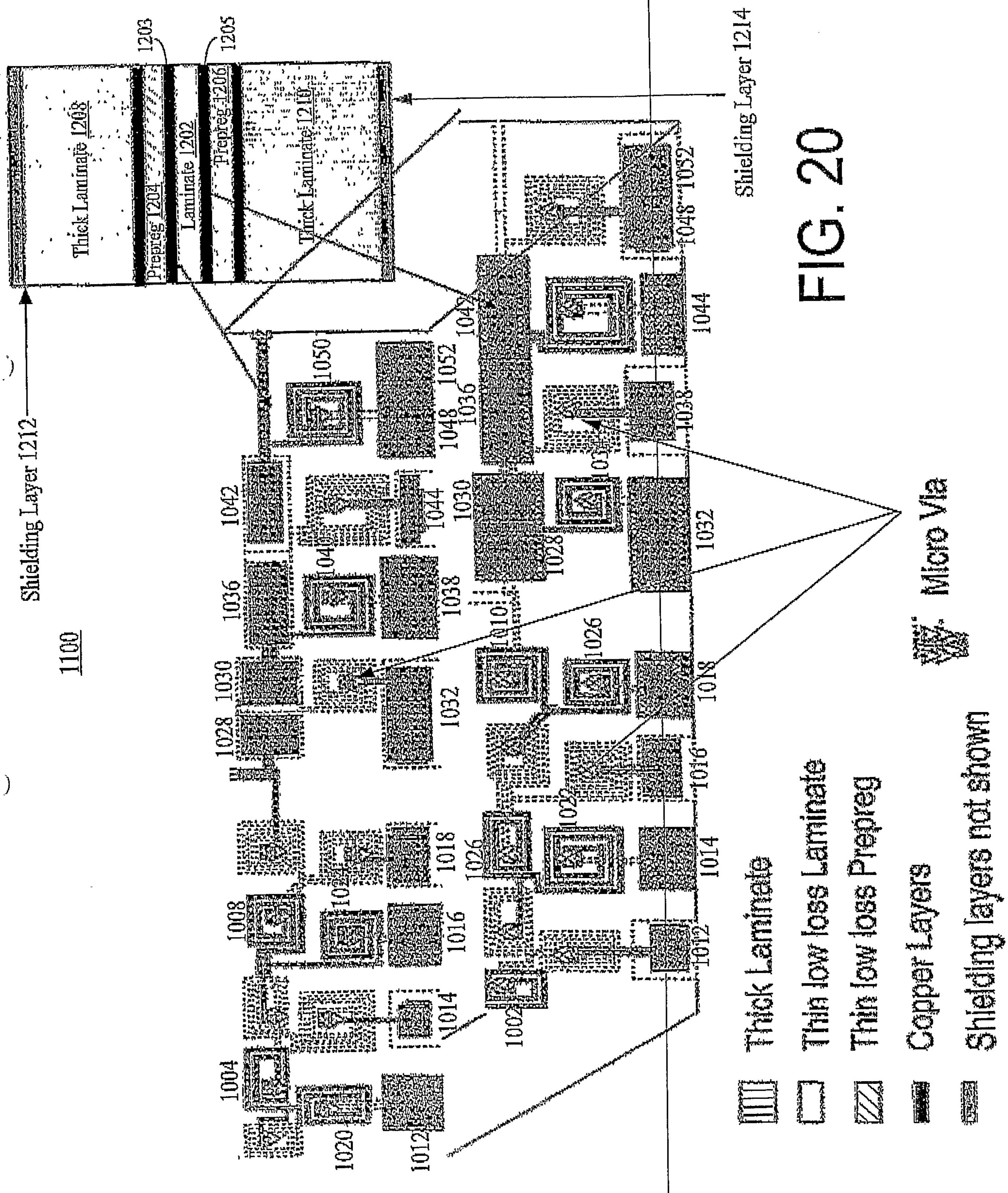

FIG. 20

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